SYNOPSYS®
Silicon to Software™

Accelerating Integration and Prototyping of IP

for Mobile and AI SoCs

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September 26th, 2019

Synopsys Contact Information

Synopsys' Website: https://www.synopsys.com/

- **DesignWare IP Subsystems**
  - https://www.synopsys.com/designware-ip/ip-subsystems.html
- **DesignWare IP Prototyping Kits**
  - https://www.synopsys.com/designware-ip/ip-accelerated/ip-prototyping-kits.html
- **FPGA Prototyping Methodology Manual**
  - https://www.synopsys.com/company/resources/synopsys-press/fpga-based-prototyping-methodology-manual.html
- **Synopsys' New HAPS-80 FPGA-Based Prototyping Solution**
  - https://www.synopsys.com/company/newsroom/mnr/synopsys-new-haps-80-fpga-based-prototyping-solution.html

Articles

- **Adaptability – Key to Fast Prototyping**
- **High-Quality Automotive IC Design with IP Subsystems**
- **Challenges of USB 3.1 IP Certification**
- **Faster Iteration Flows to Accelerate Hardware/Software Development**
- **IP Subsystems: The Next Frontier for IP Integration**
- **Accelerate Time-to-Market with Interface IP Subsystems**
- **Adapt, Port, and Integrate Quickly– Prototyping the Right Way**

For Additional Information or Contact please use this link

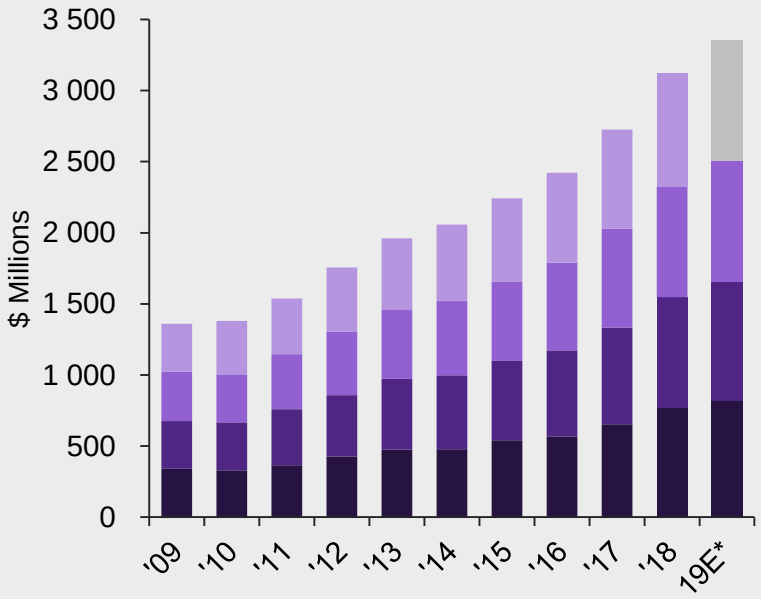
Synopsys Today: From Silicon to Software

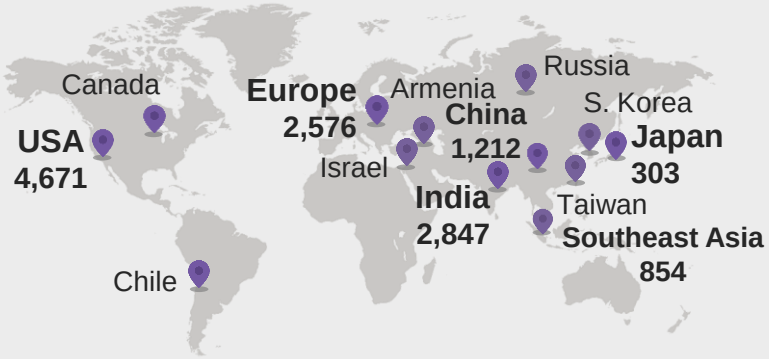
FY18 Revenue: ~$3.121B

Employees: >13,854

Patents: 3,201

Offices: 116



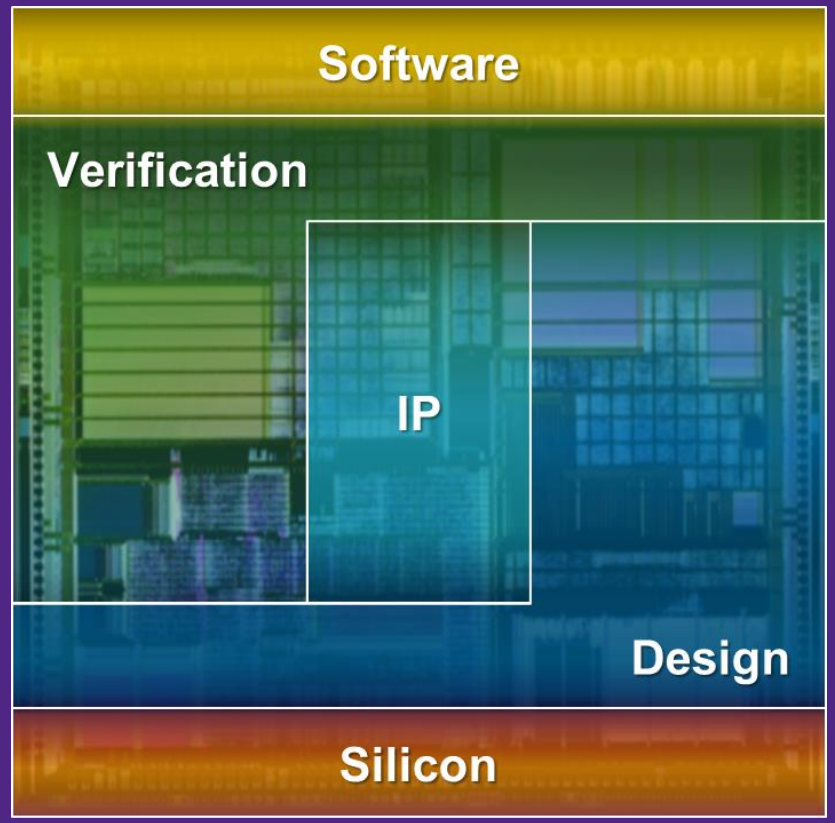


#1 electronic design automation tools & services

Broadest IP portfolio and **#1** interface, analog, embedded memories & physical IP

'Leader' in Gartner's Magic Quadrant for application security testing

Synopsys: Silicon to Software



Software
- Application security testing & quality
- Leader in Gartner's Magic Quadrant

Verification
- Fastest engines & unified platform
- HW/SW verification & early SW bring-up

IP
- Broadest portfolio of silicon-proven IP
- #1 interface, analog, embedded mem. & phys. IP

Design
- Digital & custom AMS platforms
- Best quality of results & highest productivity

Silicon
- TCAD, lithography tools & yield optimization
- Down to 5nm & below

Agenda

- What is driving today’s technological market
- The Role of Protocols and Standards as Innovation Accelerators
- Accelerating Integration – The Role of Subsystems
- FPGA Prototyping Today

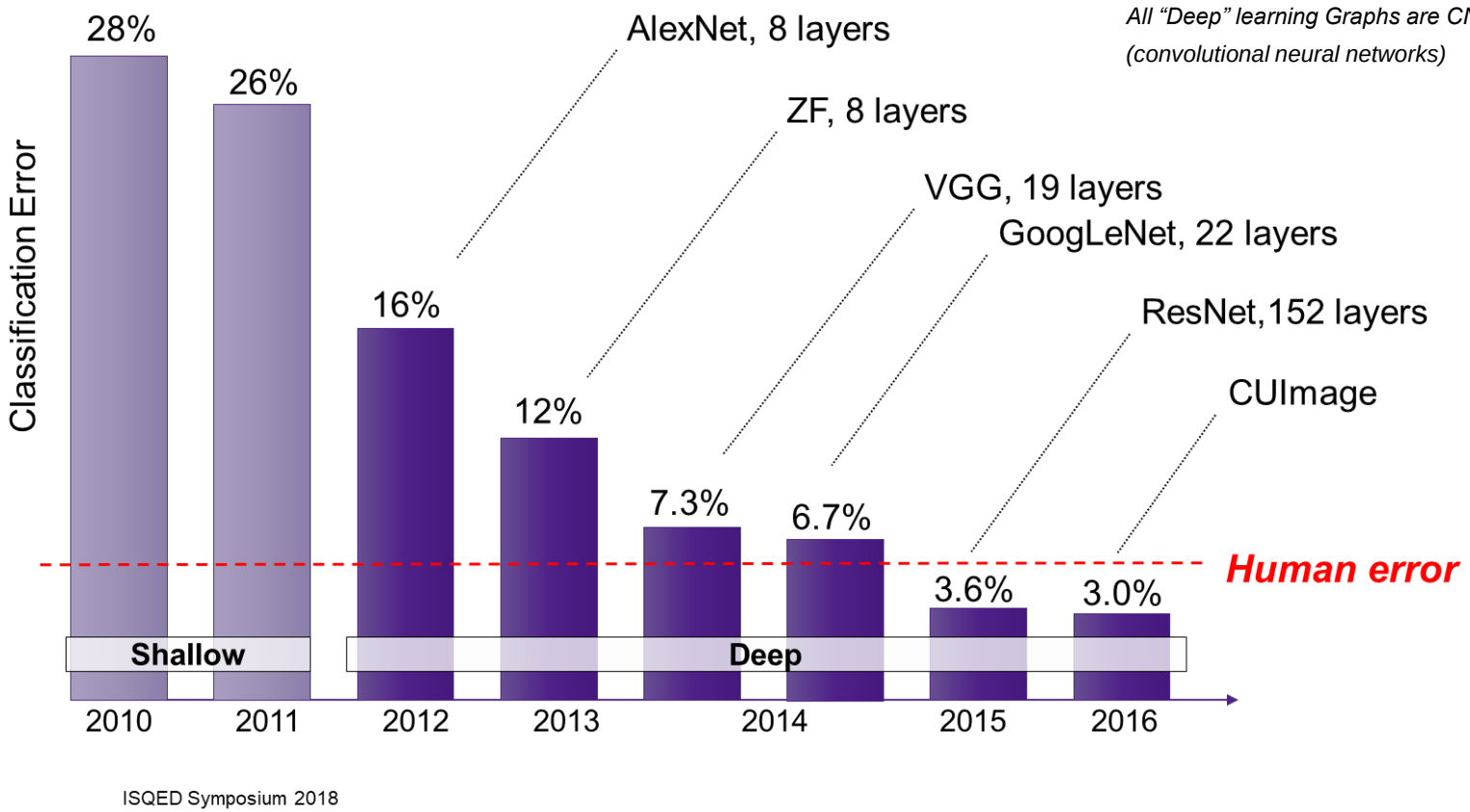
What is driving today’s technological market

AI requirements and considerations influence

What Changed the AI World

The moment in time that spurred massive AI Acceleration investment

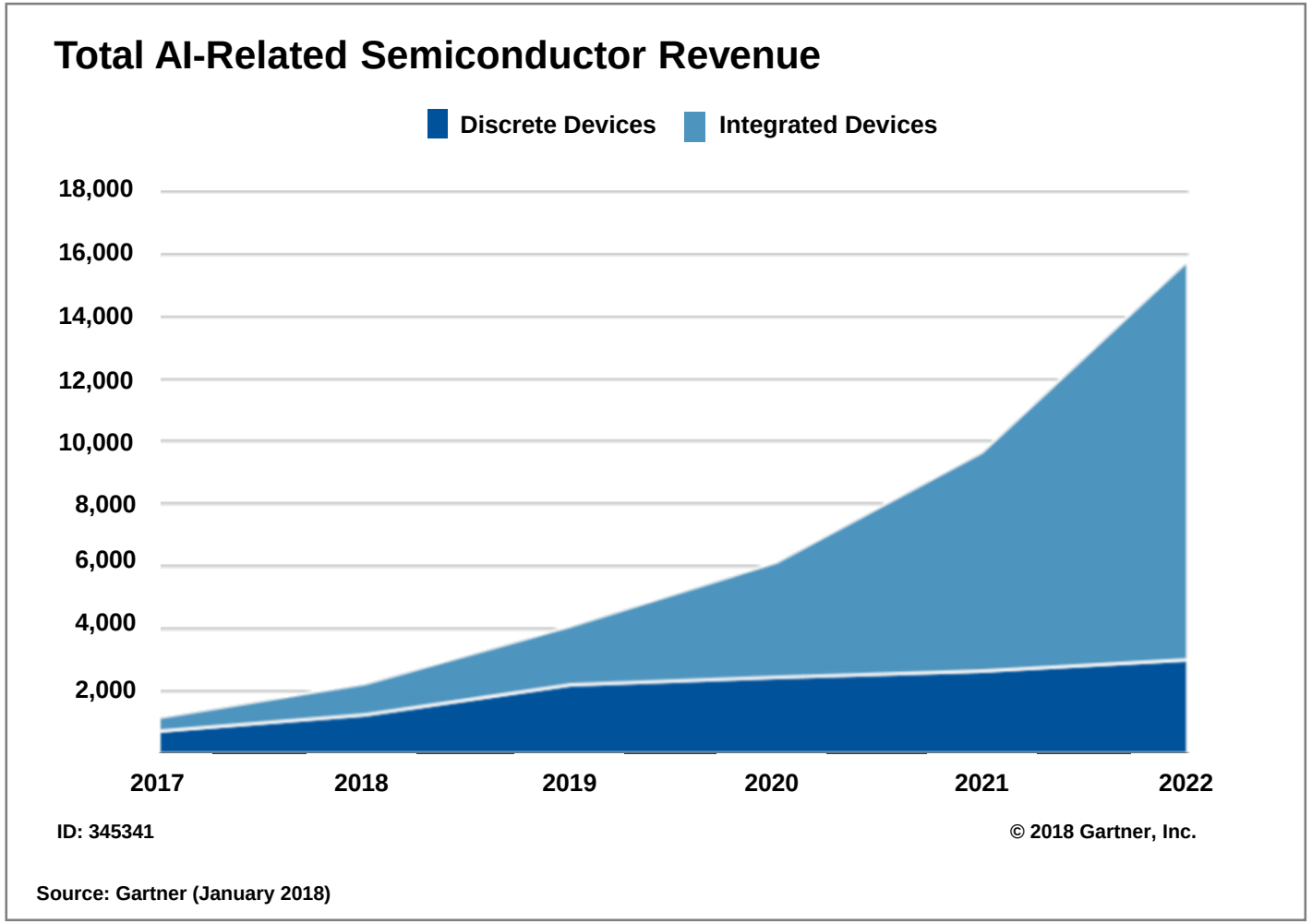
- 1986 - Geoffrey Hinton co-authored a paper on backpropagation in neural networks
- 2010 – Nvidia GeForce GTX 580 launched
- 2012 – AlexNet
  - Designed by Alex Krizhevsky
  - Published with Ilya Sutskever and Krizhevsky's PhD advisor Geoffrey Hinton
  - Running on a dual Nvidia GeForce GTX 580 GPU
  - Achieved 15.3% error at ImageNet Challenge
- 2015 – ResNet surpassed human error



ImageNet Large Scale Visual Recognition Challenge

Artificial Intelligence Market Growth

Chipsets Across all Markets will Include Deep Learning Capabilities



- Mobile - All Premier Smartphones will integrate AI Processing Capabilities by 2021
- Data Center - More than 50% of enterprises will deploy AI accelerators in their server infrastructure by 2022
- Auto - Volume production of autonomous vehicles will begin in 2020
- IoT - More than 20% of IoT devices will have AI Processing Capabilities by 2022

Gartner Jan 2018

Deep Learning SoC Challenges

Unique Requirements for Processing, Memory, Connectivity

Specialized Processing	• Heterogeneous processing (scalar, vector, neural network) • Massively parallel, matrix multiplication (neural network) • Model compression via pruning and quantization – (Increases irregular compute intensity and memory accesses)
Memory Performance	• Capacity and bandwidth constraints • Cache coherency requirements • Advanced processes maximize on-chip SRAM to reduce data movement
Real-Time Connectivity	• Reliable and configurable connectivity to AI data centers • Real-time interface to sensors, images, audio, cloud, and more • Reduced energy via power management features and FinFET technologies

Innovation in compression, lower power, less memory is required

SoC Security Design Considerations

Securing all Stages of Operation

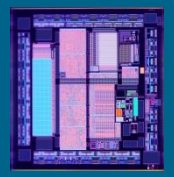
Trusted Execution Environment

Running Operation

- Continuously check for threats
- Secure communications

Powered Up

- Validate device identity
- Validate software before execution



Powered Off

- Prevent theft of stored code and data
- Protect IP

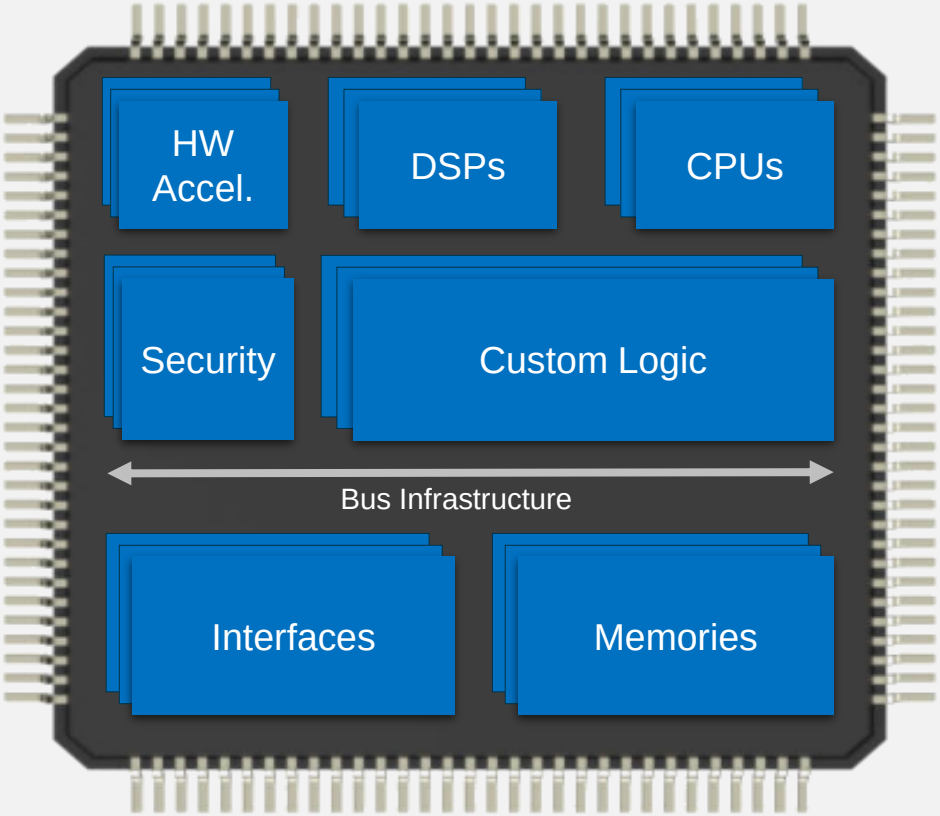
The Role of Protocols and Standards as Innovation Accelerators

Interoperability as the corner stone for ubiquitous innovation

SoC Architecture Design

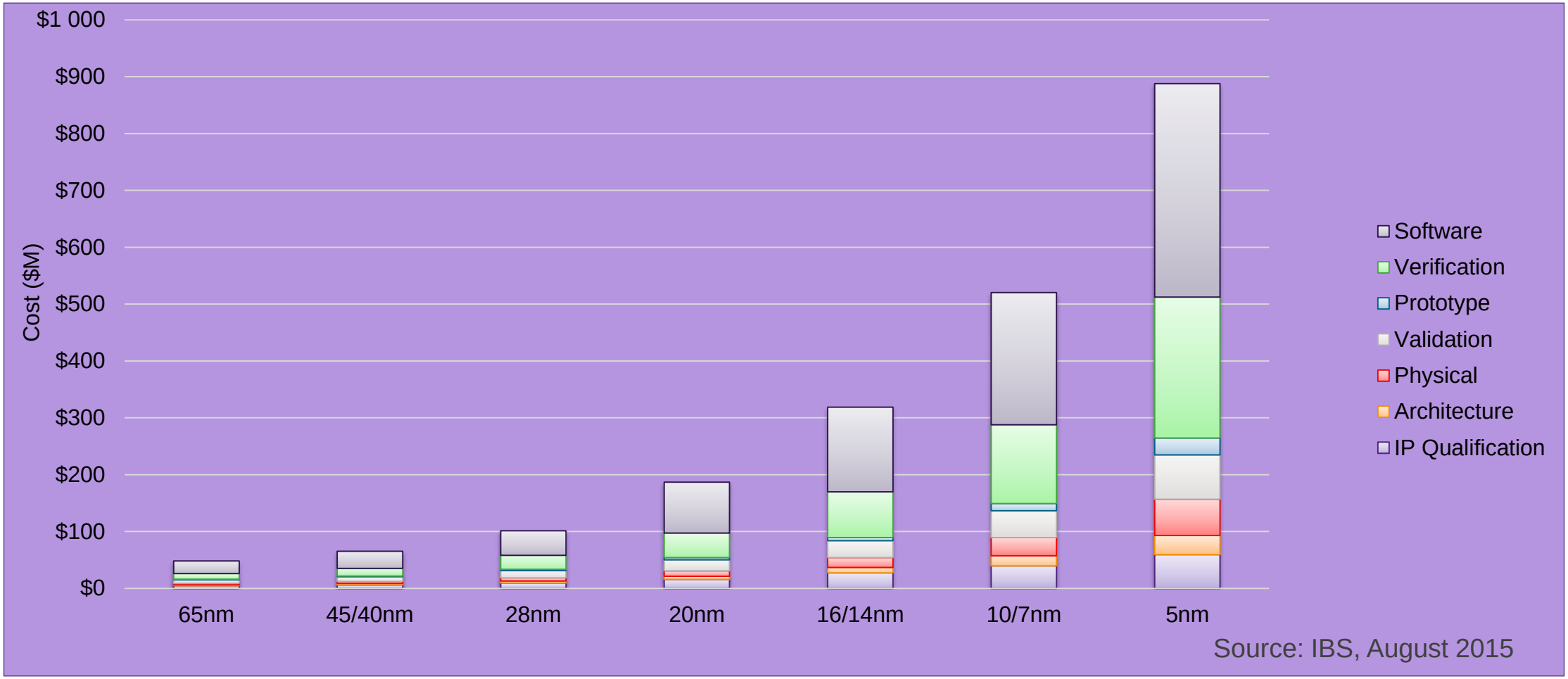
Ever growing number of considerations and challenges

- **Considerations:**
  - CPU, DSP, ASIP capabilities
  - Establish low power strategy
  - Design of key blocks (RTL, ASIP)
  - PPA (Power, Performance, Area) estimation
  - Memory architecture, bus bandwidth/latencies
  - Safety/Security considerations
  - Ensuring proper interoperability/interconnectivity
  - Verification and FPGA-based prototyping
- **How to get SoC architecture right from the start**
  - Gain confidence that PPA targets can be met without overdesign
  - Minimize course corrections to hit schedule targets
  - Hardware/Software Co-design
  - Managing TTM pressures



SoC Designs are Becoming More Complex and Costly

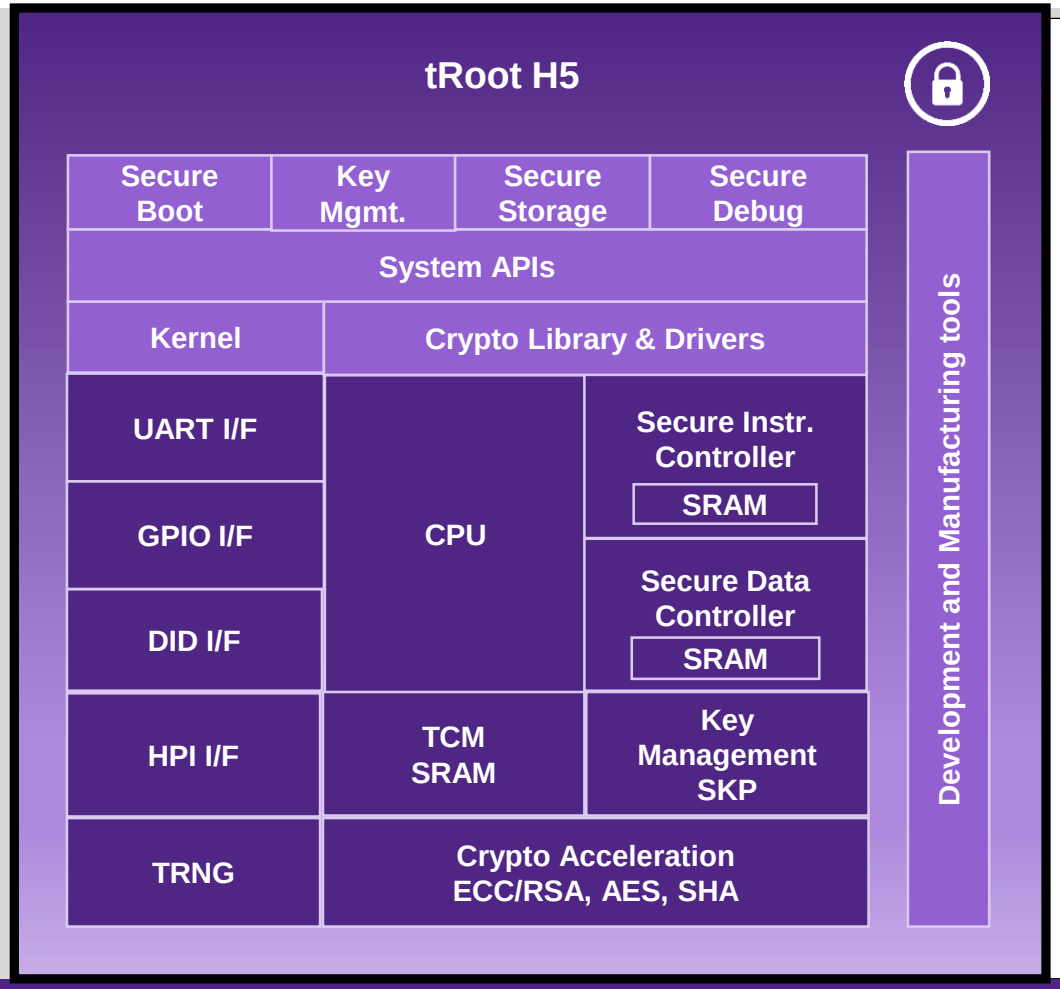
Must get the design right the first time

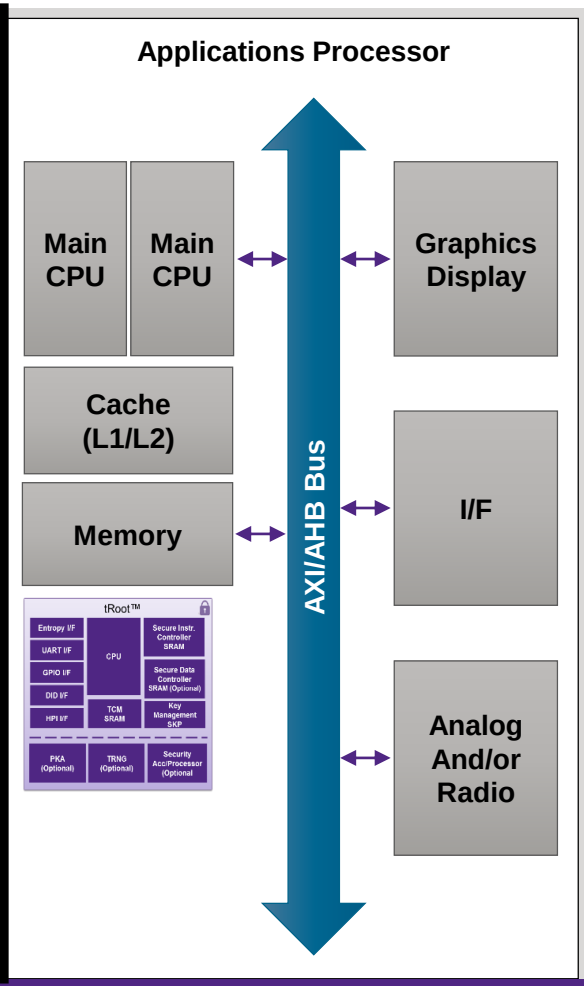


Understanding an IP

Hardware Secure Module

- Pre-built security module with a unique ID that cannot be tampered with
- Provides robust security functionality
- Extends security to other internal and external entities in an SoC
- Pre-defined security perimeter
  - Reduces security knowledge requirements
  - Lowers design risks
  - Accelerates time to market

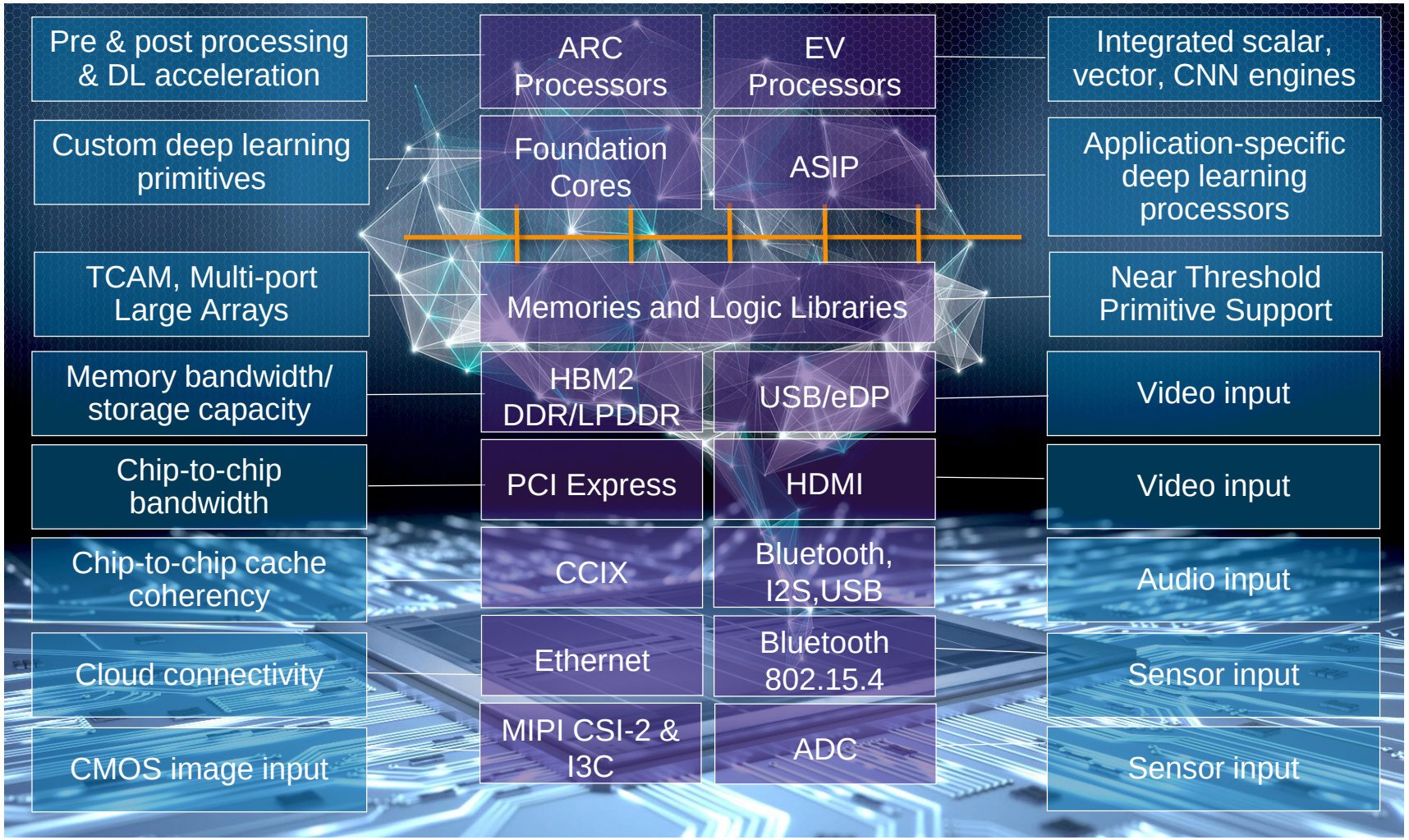




Secure Module Enables Implementation of Trusted Execution Environments

DesignWare IP for AI

Building Innovative Deep Learning SoC Designs

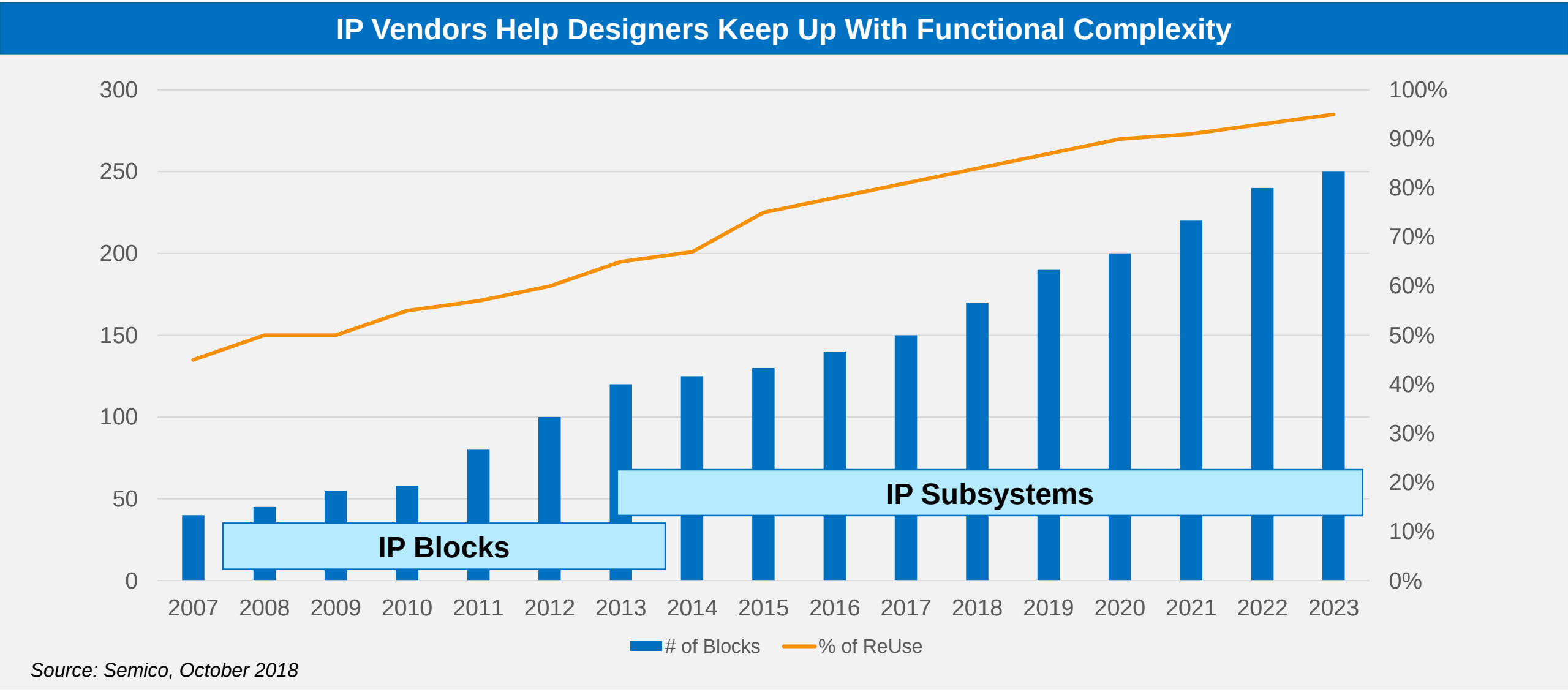


- ARC & EV Processors, ASIP Designer, and Foundation Cores for specialized processing
- DDR, HBM2, CCIX, Embedded Memories and Logic Libraries for optimized memory performance
- Portfolio of silicon-proven interface IP for real-time data connectivity

Accelerating Integration – The Role of Subsystems

Focusing in Added Value and Differentiating factors, instead on the building blocks

Silicon IP Trends: IP Blocks → Subsystems (HW + SW IP)

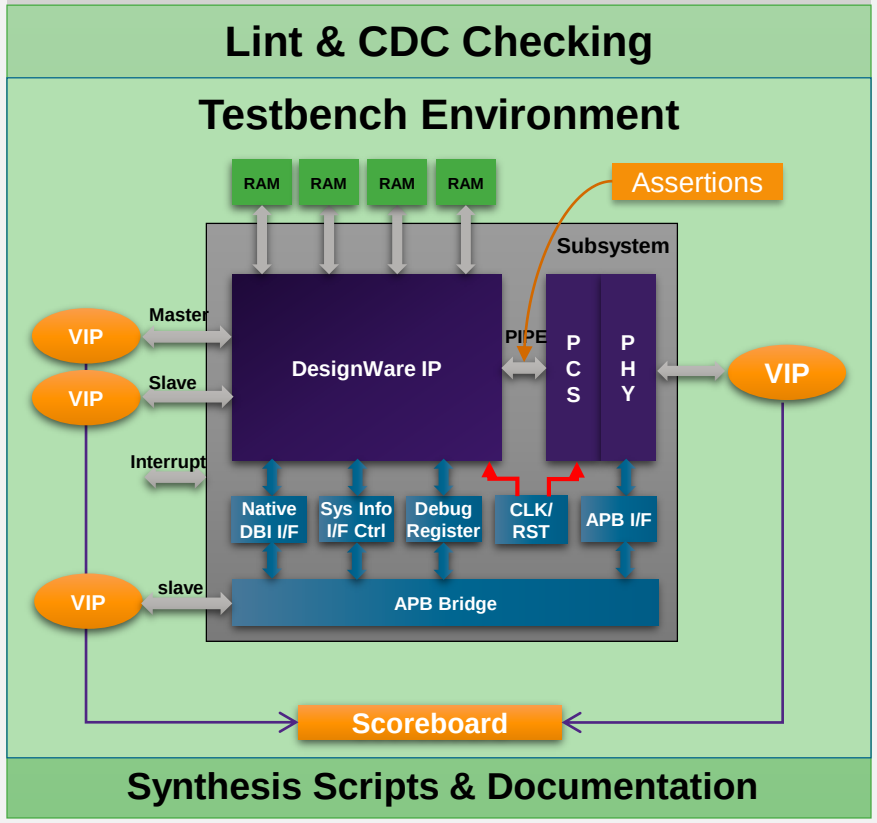


Source: Semico, October 2018

IP Subsystems: More than Controller + PHY

Specific to Your Application & SoC

SoC Experts + IP Experts =
Fastest Integration of IP into your SoC

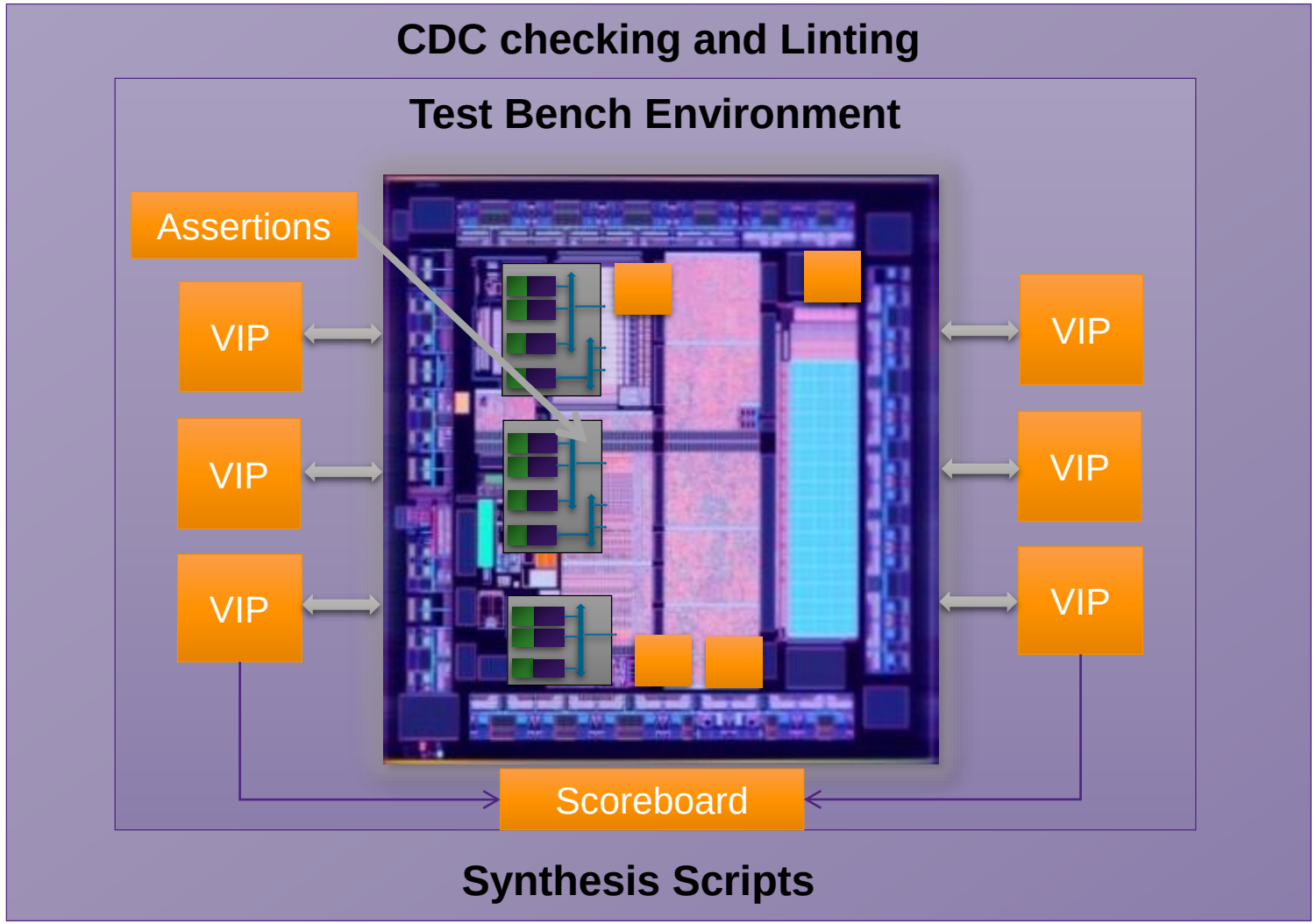


Minimize integration effort, reduce overall development cost, and meet critical project schedules

- **Built by Protocol experts & customized to exact requirements**
  - Incremental deliverables throughout project
- **Comprehensive subsystem level verification**
  - Comprehensive end-to-end suite of tests, reusable at SoC
- **Subsystem analysis**
  - Lint and CDC/RDC checking
  - Timing analysis with SoC-specific technology library
- **Synthesis scripts & comprehensive integration documentation**
- **Optional Extra value: DFT, SRAM integration, BIST**

Comprehensive Testing and Scripts for SoC Integration

Fastest SoC Integration



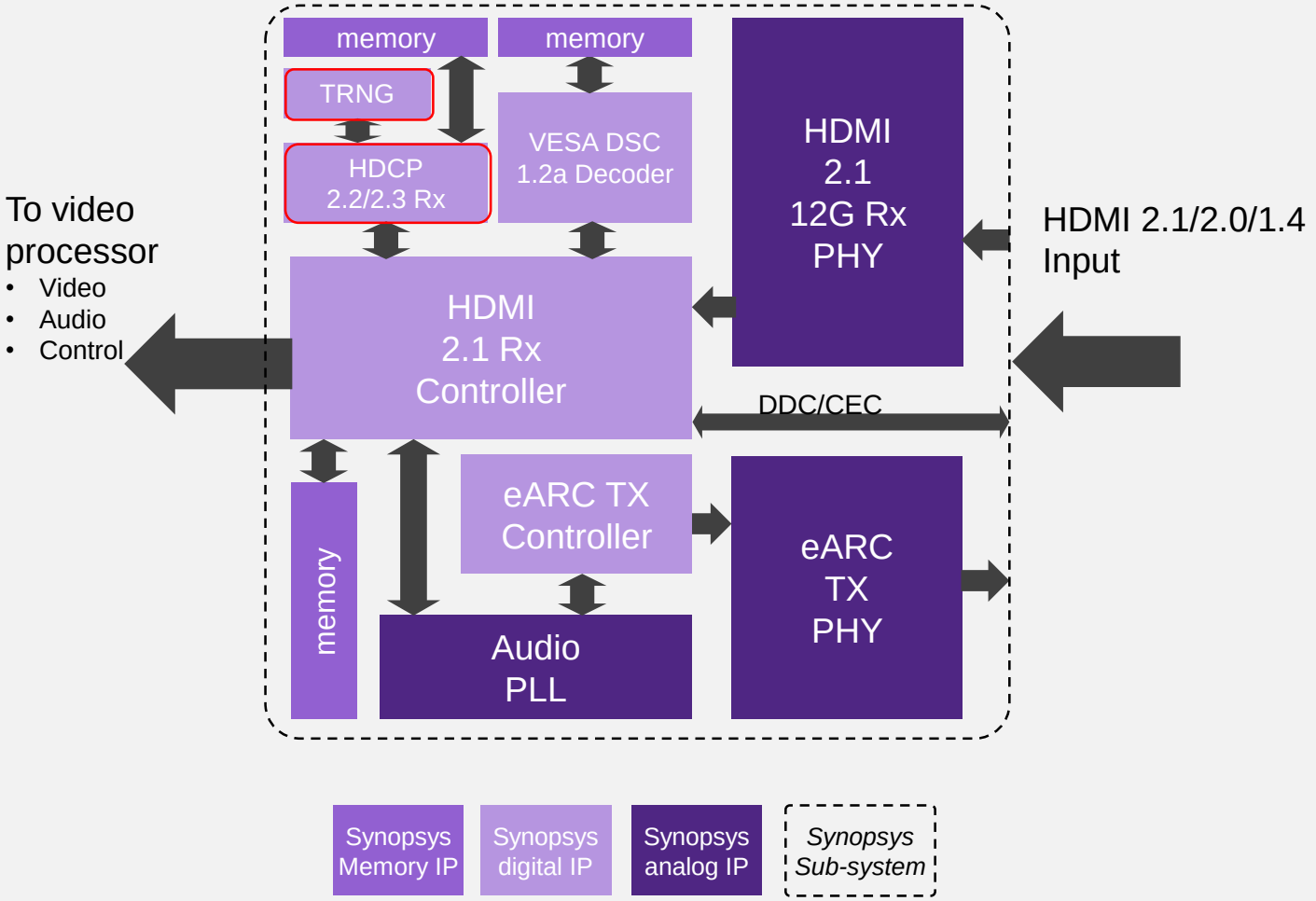
- Easy & Rapid Integration into SoC environment
- Fully documented
- Direct Support

Documentation

- Functional specification
- Verification plan and programming guidelines
- Implementation guidelines

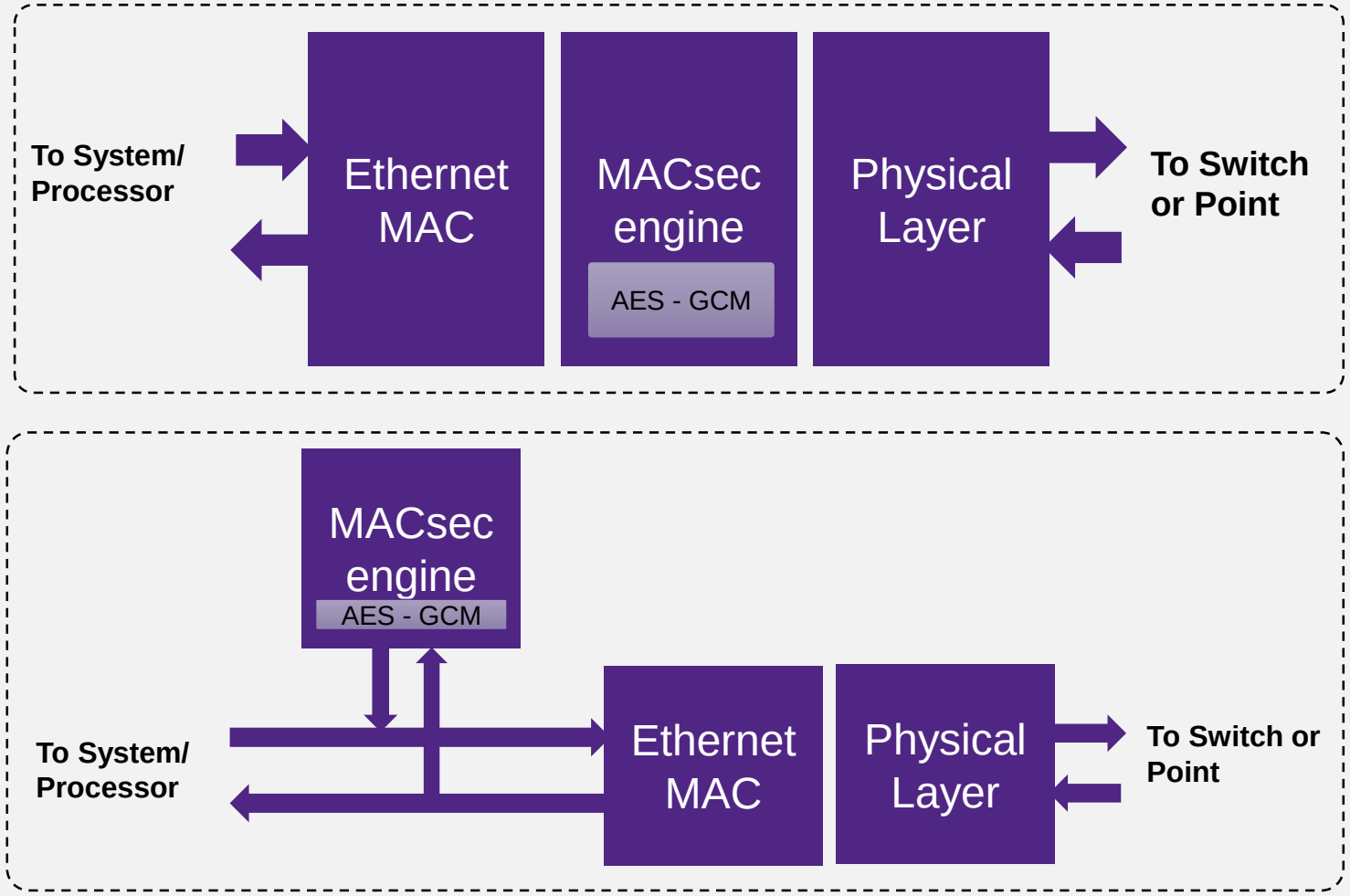
HDCP used in HDMI RX Applications

Synopsys HDMI RX Subsystem Showing HDCP and TRNG



- TRNG typically used in rest of system and not included at this level
- HDCP is required for secure content
- Multi-port HDCP for fast switching in multi-port RX applications

MACsec Engine as a In-Line or Look-Aside Accelerator

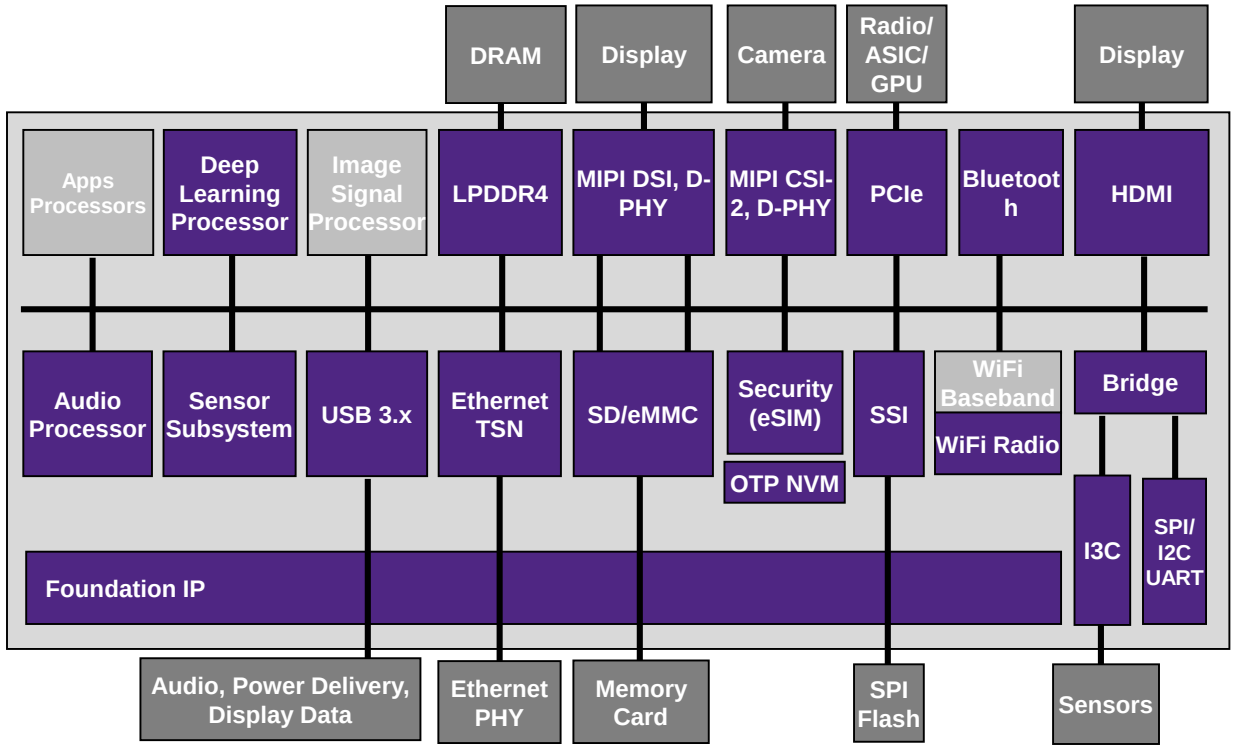


- Typical implementation
- Low latency
- Can be disabled for non-secure applications or key only data validation

- Some advantages
  - Saves gates in Multi-Port System
  - Easier to implement where MAC and PHY are tightly coupled

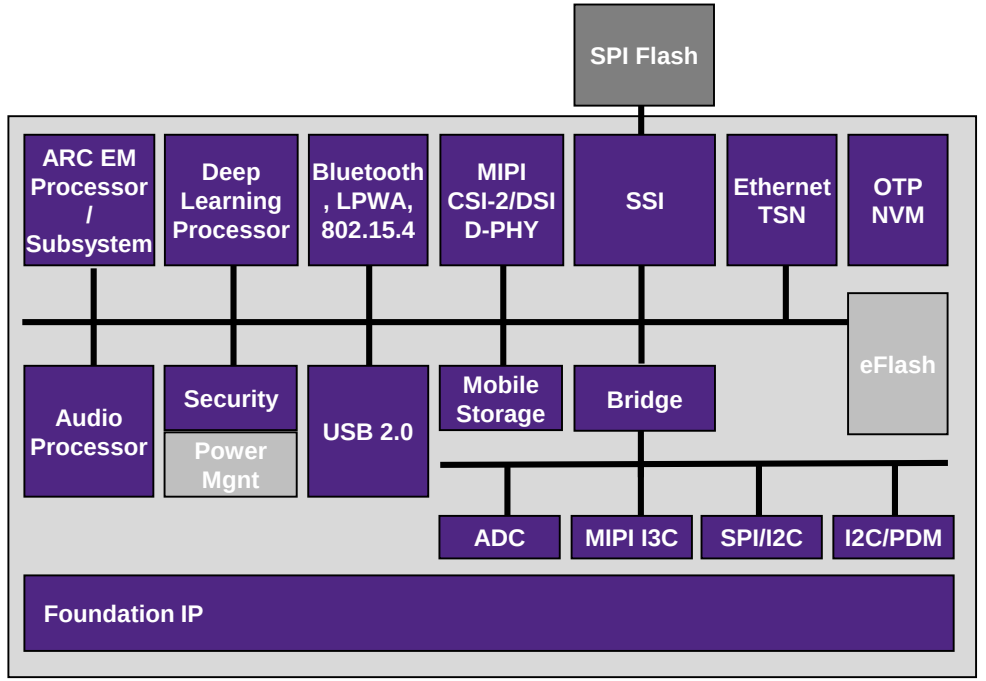
Digital Home and IoT Edge SoC Architectures

Digital Home/IoT (Edge)



22-, 12-nm
Security cameras, digital home, drones

Low-End IoT (Edge)



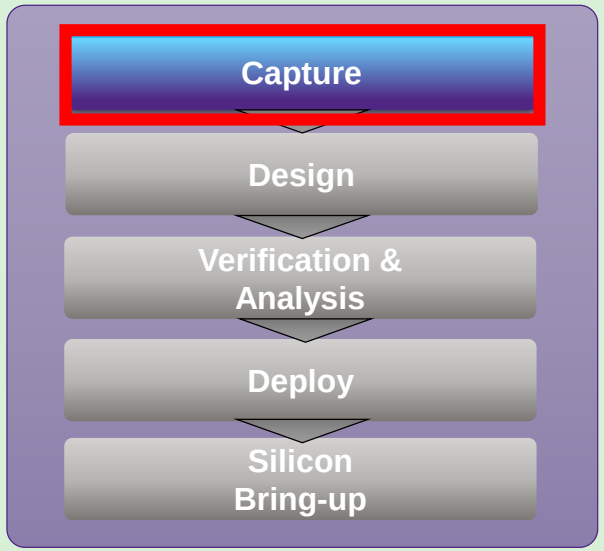
90-, 55-, 40-nm, next-generation 40-, 22-nm
Voice/NLP/NLU, facial detection, human activity activation, audio

CoStart with IP Subsystems Experts

Reduce Design Risk with Architectural Consultation and Design of Subsystem

Reduce Design Risk

- IP & SoC experts configure and customize to your requirements
- Frees your team to work on your product differentiation



Architectural Consultation

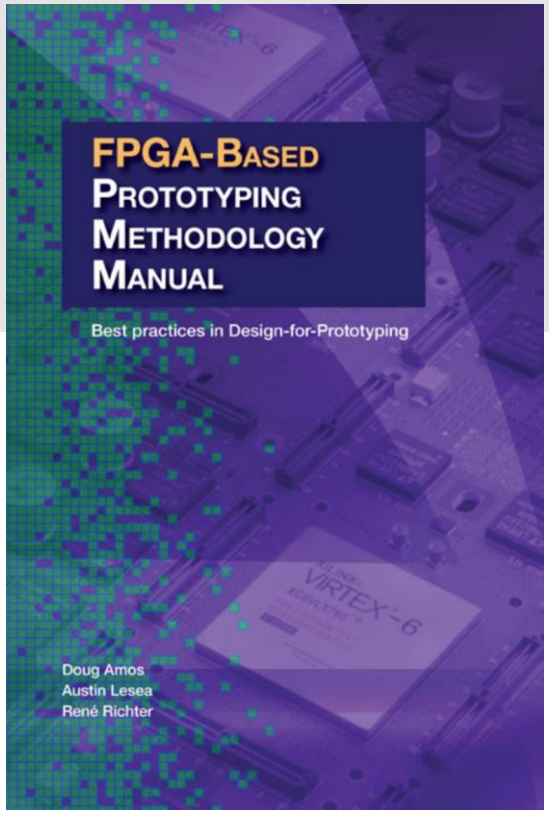
- **Rapid Translation of SoC Requirements to Subsystem**
  - Focused on Architecture, Specific Features, Performance, Clocking
- **Deliverable: Functional Specification Document**
  - Configuration
  - IP Subsystem Architecture
  - Clocking/Reset Architecture
  - Additional Custom Blocks

Accelerate Time-to-Market

- First-time-right integration speeds TTM

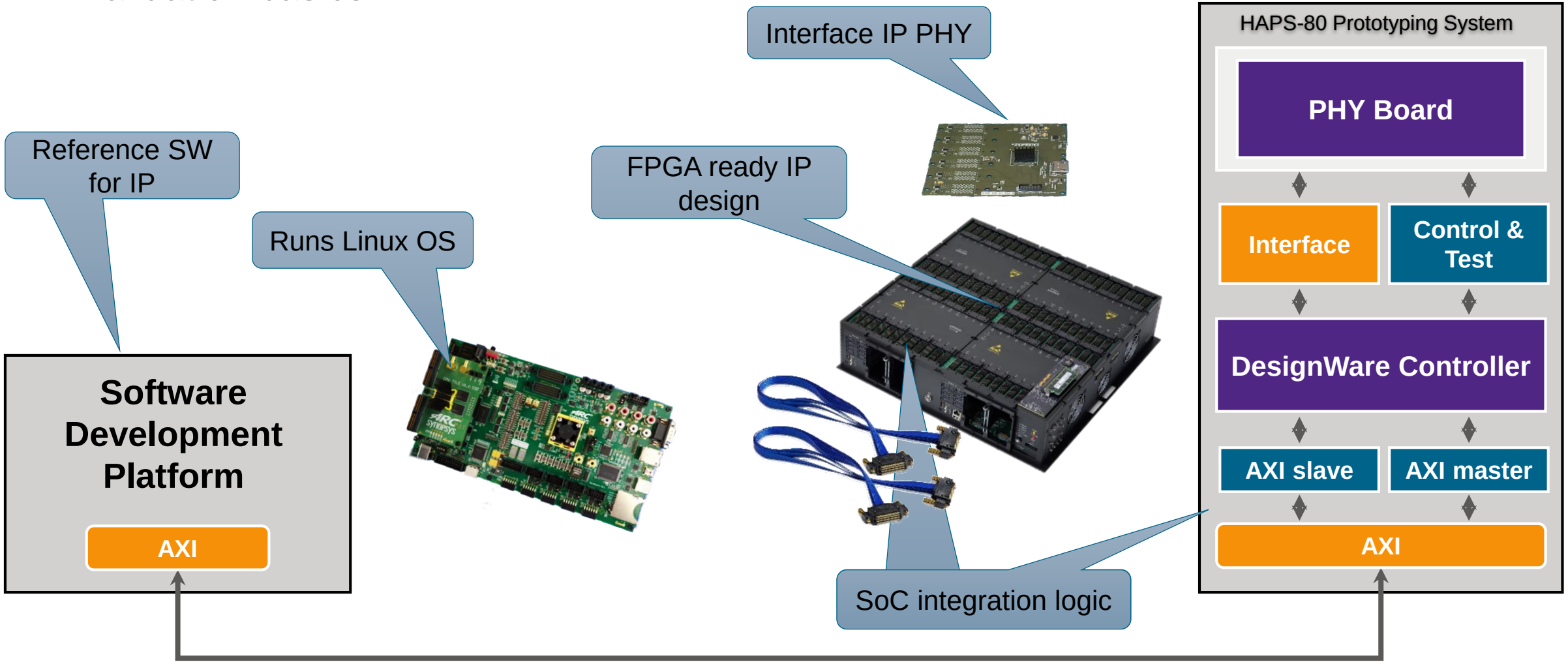
FPGA Prototyping Today

From the single FPGA board to a scalable every increasing resource/frequency solution



How to Prototype an IP Subsystem

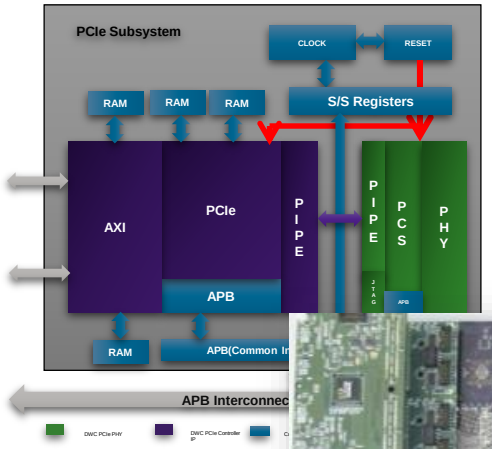
IP Validation basics

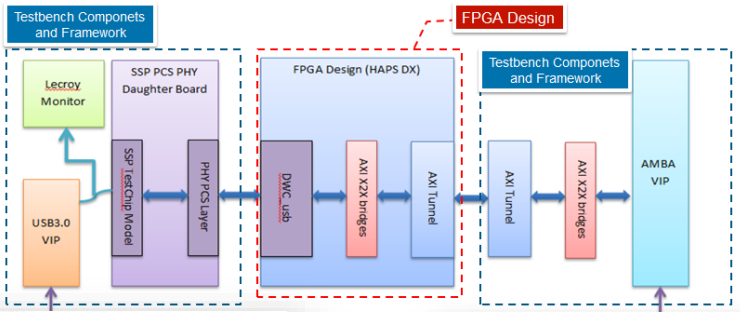


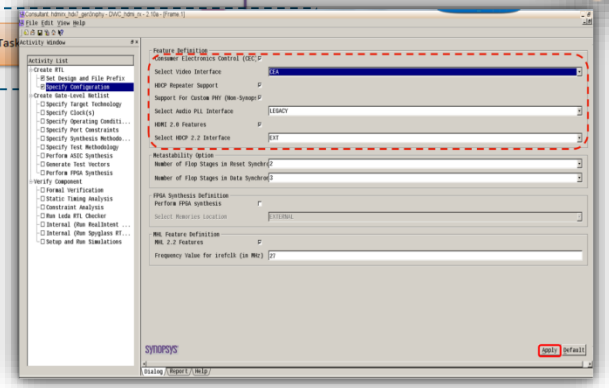
Improve IP Prototyping Schedule

Cuts Months from Integration, Prototyping and SW Schedule

Create IP Reference Design	Create Board & PHY Daughter card	Validate Reference Design	Explore IP Configuration	Firmware, driver, bootcode development







Hardware/Software Validation

Validation of HW & SW in concert with the real world

- System validation: Test final product use-cases
  - Full protocol stack
  - Digital (RTL), analog (PHYs), Software
- Goal: Uncover corner case faults
  - Using real world scenarios (IO)
  - Using production software images
- Focus:
  - Software & hardware defects
  - Interoperability issues
  - Performance flaws

360 Camera Example

Hardware/Software Validation

Typical faults found during system validation

- Software:
  - Driver issues abstracted in PHY models
  - Corner case defects in long scenarios (e.g. Protocol flaws)
- Performance:
  - Unexpected contention, latencies due to integration of all subsystems
  - Missed real-time requirements discovering SW malfunctions (deadlocks, timeouts)
- Hardware Interoperability:
  - Signal integrity
  - Protocol completeness & robustness
  - Specification interpretation
- System Power Management:
  - Power-up/down sequence deadlocks

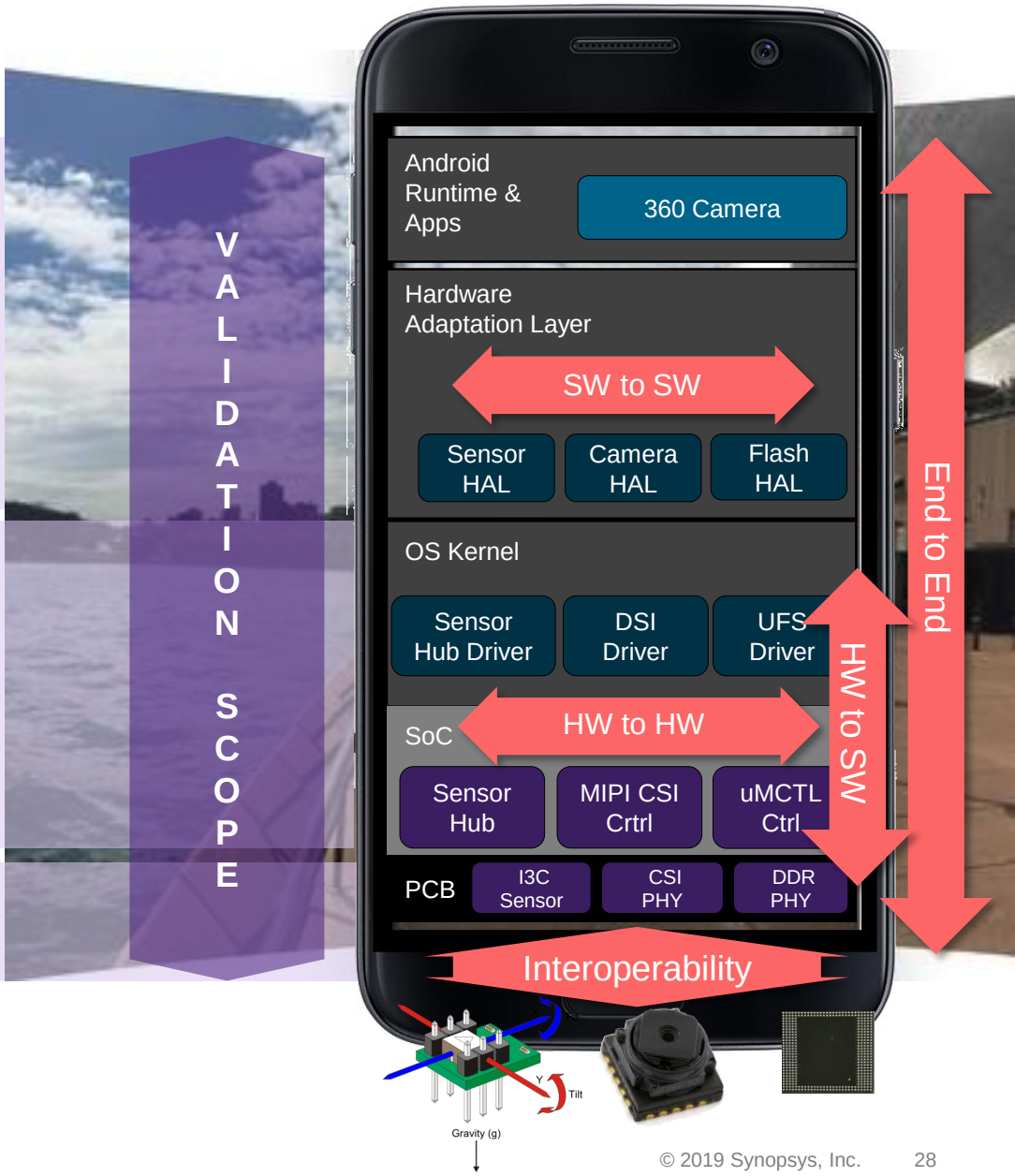
Applications, Benchmarks, Compliance Tests

Protocol Standard

Physical Standard

VALIDATION SCOPE

360 Camera Example



Hardware/Software Validation

Validation of HW & SW in concert with the real world

- System validation requires:
  - ASIC RTL
  - Real world interfaces (PHYs)
  - Connected ICs/devices
  - Production software
  - Close to real-time performance
  - System-level observability for failure analysis
- HAPS Prototyping
  - Highest capacity & performance multi-FPGA systems
  - Comprehensive clock infrastructure and SW flow
  - Large portfolio of PHY daughter boards & complete IP kits
  - Widely deployed in the industry for system validation

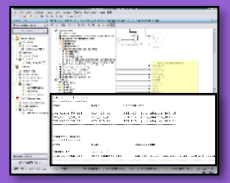
360 Camera Example

Hardware/Software Validation

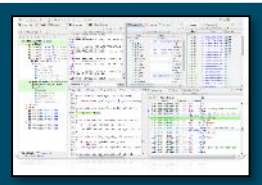
HAPS Prototyping Solution

ASIC Design (RTL)

Daughterboards definition/ IP Prototyping Kits

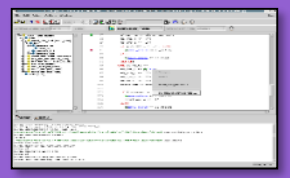


Create FPGA bitfile(s) with HAPS ProtoCompiler

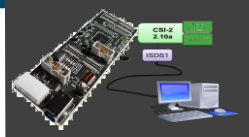


Software Debugger

HAPS-80 System



HW debug with ProtoCompiler Debug



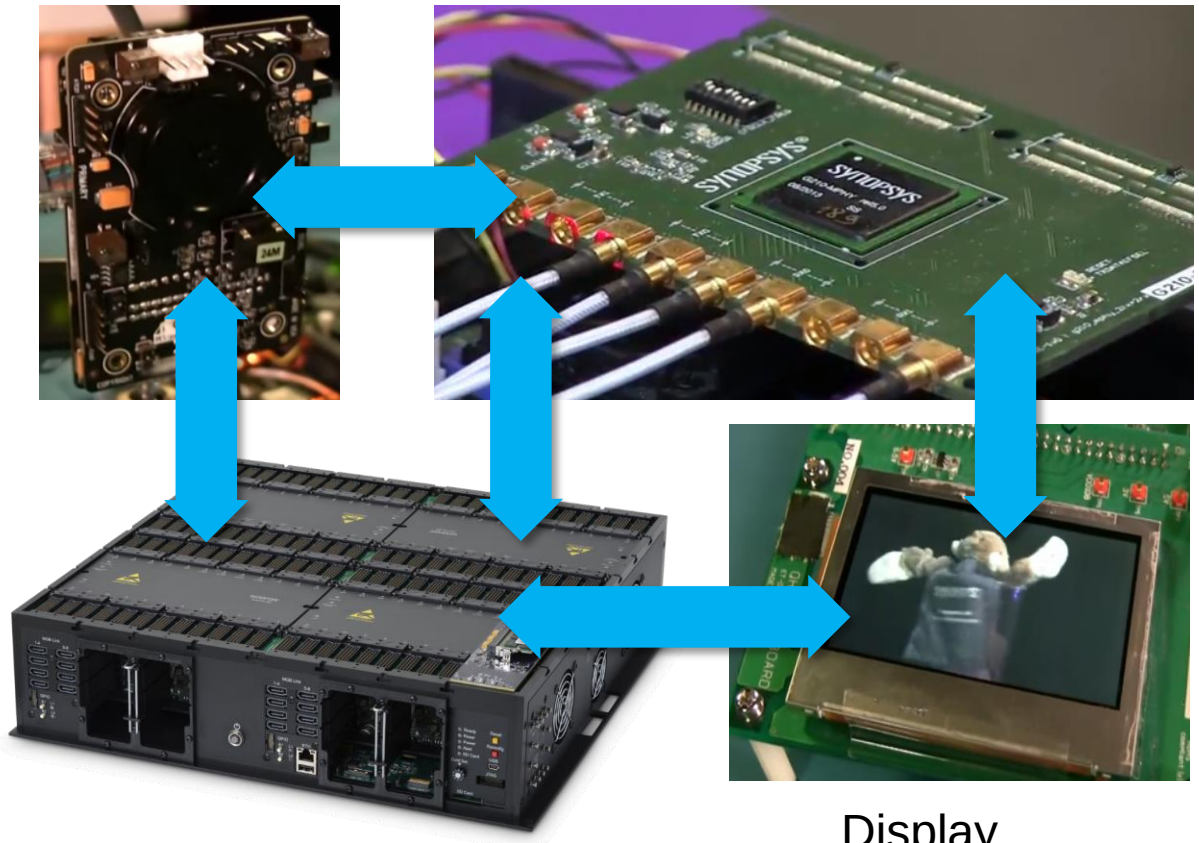
PHY daughterboards IP Prototyping Kits

Hardware/Software Validation

HAPS Prototyping Solution

Camera

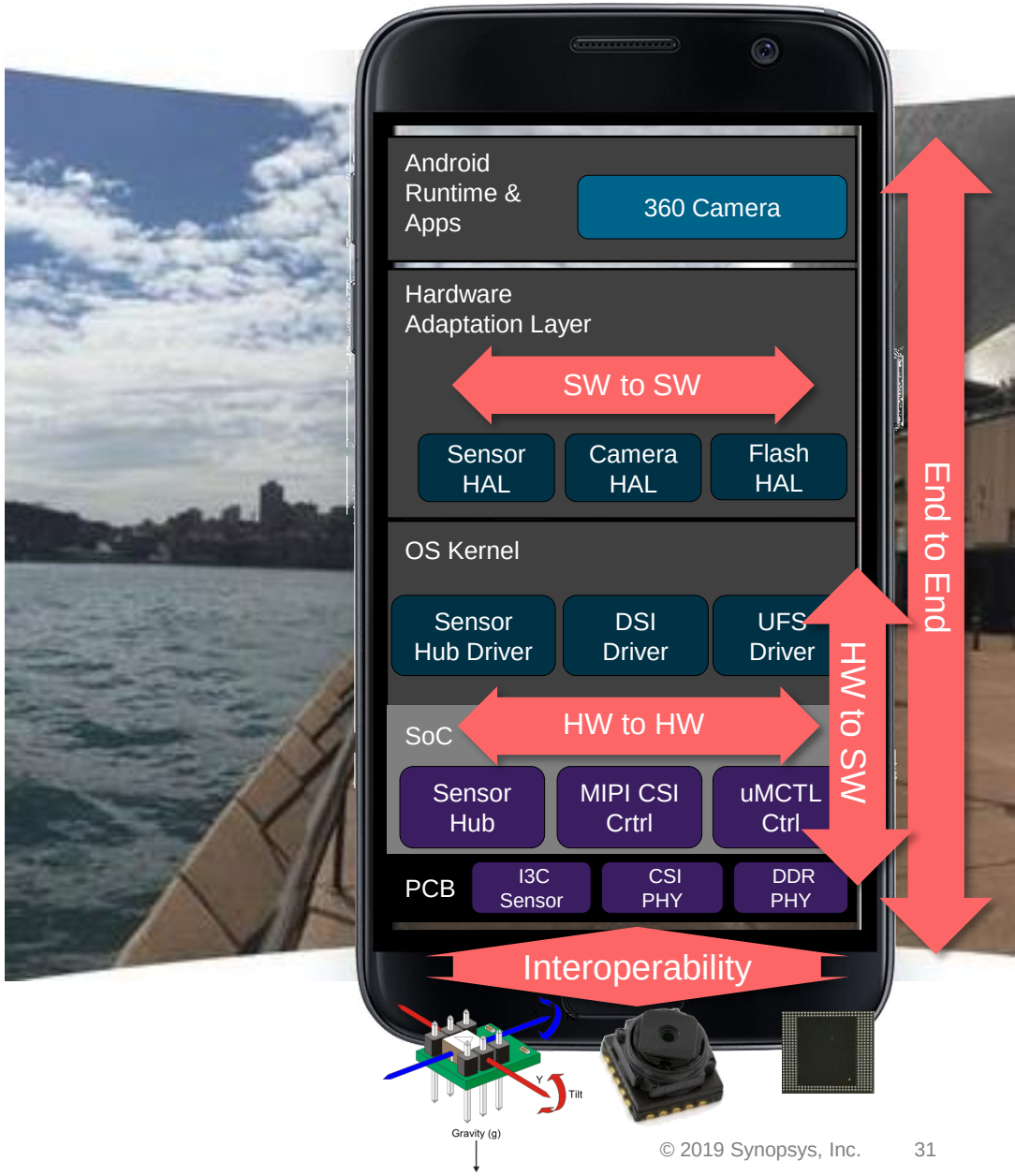
MIPI PHYs



HAPS-80 System

HapsTrak 3 PHY Daughter boards

Display



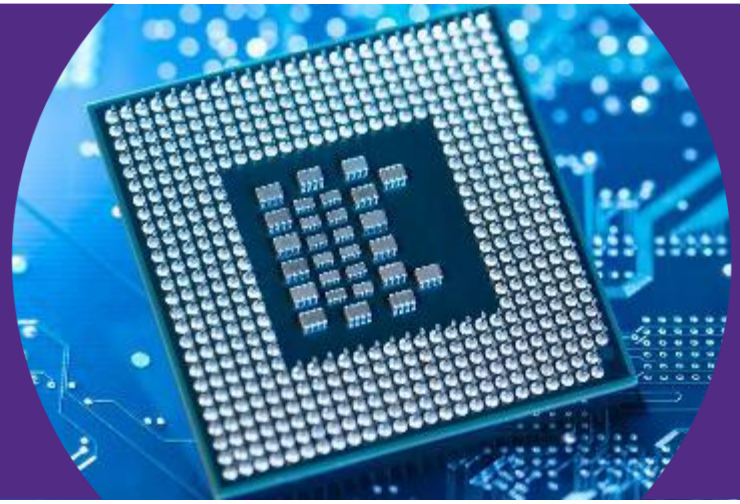
IP Prototyping Kits Accelerate Integration

Cuts Months from Integration, Prototyping and SW Schedule

Synopsys Provides Solutions

IP Accelerated

DesignWare IP
Tuned to Your SoC



Hot Markets

Automotive, ML,
Cloud, 5G, IoT

Processors EV6x, HS, EM	**Security IP** tRoot, HDCP 2.3, Provisioning	**High Speed Data Converters** 3Gbps/6Gbps	**Logic Libraries/ Embedded Memories**	**NVM** OTP, MTP	**Process Technologies** FinFET (7/5/4nm) Planar (22nm…)
USB 3.1 Type-C w/DP, USB 3.2, eUSB, USB4	**DDR** DDR5 (4800), LPDDR5 (6400), HBM2E (3200)	**PCI Express** PCI Express 5.0, CCIX, CXL, LP PCIe 4.0	**Multi-Protocol SerDes** 56G/112G	**HDMI** v2.1TX/RX	**MIPI** D-PHY 2.1, UFS 3.0, C/D-PHY

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