

Call for Contributions

Inform the Chair: With the Title of your Contribution

Submission URL:

<https://www.iariasubmit.org/conferences/submit/newcontribution.php?event=DEPEND+2017+Special>

Please select Tract Preference: HP-DoCNet

Special Track

HP-DoCNet: High Performance and Dependable on-Chip Networks

Chair and Coordinator

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along with

DEPEND 2017, The Tenth International Conference on Dependability

September 10 - 14, 2017 - Rome, Italy

<http://www.aria.org/conferences2017/DEPEND17.html>

The growth in number of transistors with technology has propelled the integration of several processing elements onto a single silicon chip, a.k.a. System-on-Chip (SoC). To compensate for this fast-paced technological scalability with the performance bottleneck of conventional bus-based interconnect, Network-on-Chip (NoC) has emerged as an alternative on-chip communication platform that facilitates the integration of novel interconnect fabrics such as optical networks, three-dimensional integrated circuits (3D ICs) and millimetre-wave (mm-wave) for emerging SoC design. Several research efforts have been made to mitigate the performance and manufacturing cost in terms of silicon area, power consumption, reliability, latency and throughput of the NoC. However, merely metal-based interconnect stretches performance limits under the continuous and relentless technology scaling which calls for on-going investigation and development in this field.

This track on the High Performance and Dependable on-Chip Networks (HP-DoCNet) will represent an international forum for researchers from both academia and industry to present the latest trends, research findings, and emerging issues in this area.

Topics include, but not limited to:

- Wireless NoC, RF NoC, Surface-Wave NoC, Optical NoC
- Three-dimensional Network-on-Chip (3D NoC)
- Technology constraints on NoCs
- Router microarchitecture
- Flow control techniques; Switching techniques; Routing Algorithms
- Optimization techniques
- Fault tolerance/reliability in NoC
- Technology constraints on NoCs
- Scheduling and application mapping onto NoCs
- NoCs scalability, modeling and performance evaluation
- FPGA-based implementation of reconfigurable NoCs

Important Dates:

- **Inform the Chair:** As soon as you decide to contribute
- **Submission: August 2, 2017**
- Notification of Acceptance: August 9, 2017
- Registration: August 16, 2017

Note: These deadlines are somewhat flexible, providing arrangements are made ahead of time with the chair.

Contribution Types

- Regular papers [in the proceedings, digital library]
- Short papers (work in progress) [in the proceedings, digital library]
- Posters: two pages [in the proceedings, digital library]
- Posters: slide only [slide-deck posted on www.iaia.org]
- Presentations: slide only [slide-deck posted on www.iaia.org]
- Demos: two pages [posted on www.iaia.org]

Paper Format

- See: <http://www.iaia.org/format.html>
- Before submission, please check and comply with the editorial rules: <http://www.iaia.org/editorialrules.html>

Publications

- Extended versions of selected papers will be published in IARIA Journals: <http://www.iaiajournals.org>
- Print proceedings will be available via Curran Associates, Inc.: <http://www.proceedings.com/9769.html>
 - Articles will be archived in the free access ThinkMind Digital Library: <http://www.thinkmind.org>

Paper Submission

<https://www.iaiasubmit.org/conferences/submit/newcontribution.php?event=DEPEND+2017+Special>

Please select Track Preference **HP-DoCNet**

Registration

- Each accepted paper needs at least one full registration, before the camera-ready manuscript can be included in the proceedings.
- Registration fees are available at <http://www.iaia.org/registration.html>

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